Docket No.: M4065.135/P135
Micron Ref.: 98-0673

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

# METHOD OF FORMING A METAL SEED LAYER FOR SUBSEQUENT PLATING



Inventors:

**Terry L. Gilton**
**Dinesh Chopra**

Dickstein, Shapiro, Morin &
Oshinsky LLP
Suite 400
2101 L Street, N.W.
Washington, D.C. 20037
(202) 785-9700

# METHOD OF FORMING A METAL SEED LAYER FOR SUBSEQUENT PLATING

## FIELD OF THE INVENTION

The present invention relates to the field of electrochemical deposition, and in particular to a method of forming a metal seed layer by electroplating.

## BACKGROUND OF THE INVENTION

The performance characteristics and reliability of integrated circuits have become increasingly dependent on the structure and attributes of the vias and interconnects which are used to carry electronic signals between semiconductor devices on integrated circuits or chips. Advances in the fabrication of integrated circuits have resulted in increases in the density and number of semiconductor devices contained on a typical chip. Interconnect structure and formation technology has lagged behind these advances, however, and is now a major limitation on the signal speed of integrated circuits.

Current techniques for forming vias and interconnects begin with preparation of the semiconductor wafer surface by formation of an interlevel dielectric layer (ILD), typically silicon dioxide. A mask may then be applied to pattern the deposition of the interconnect material on the wafer in the desired manner. Another typical process is to plate the interconnect material onto the surface of the wafer to a depth sufficient to fill the vias, followed by planarization to achieve the desired interconnect pattern.

Typically the preferred metal for use in the construction of integrated circuit interconnects has been aluminum. Aluminum is widely used because it is inexpensive, relatively easy to etch, and adheres well to ILDs such as silicon dioxide. Disadvantages of aluminum include significant electromigration effects,

susceptibility to humidity-induced corrosion, and the tendency to "cold creep". "Cold creep" is a process that creates cracks or spaces between the interconnect layer and the ILD due to large variances in the coefficient of thermal expansion between the two materials.

The disadvantages of aluminum interconnects have become more pronounced as the geometry of integrated circuits continues to shrink. Chip designers have attempted to utilize different materials to construct an interconnect system having the chemical and mechanical properties which will complement and enhance smaller and faster circuit systems. The ideal interconnect material is inexpensive, and has low resistivity, minimal electromigration effects, high corrosion resistance, and a similar coefficient of thermal expansion to the ILD and substrate material. Metals possessing these properties include gold, silver, and copper, and research has generally focused on these three metals as new via and interconnect materials.

Copper is the most attractive material for use in integrated circuits because of its desirable chemical and mechanical properties. It is an excellent conductor with a resistivity of 1.73 microOhms per centimeter, is inexpensive, and is easily processed. Copper also has fewer electromigration effects than aluminum and can therefore carry a higher maximum current density, permitting a faster rate of electron transfer. The high melting point and ductility of copper produce far less cold creep during the semiconductor fabrication process than many other metals, including aluminum.

Although copper has many favorable characteristics, it also has disadvantages that may create fabrication problems for chip designers. Copper is soluble in silicon and most common ILDs, and exhibits a high rate of diffusion at temperatures associated with integrated circuit manufacturing. This diffusion can

result in the creation of intermetallic alloys which can cause malfunctioning of the active semiconductor devices. In addition, copper exhibits poor adhesion to silicon dioxide which can result in broken connections and failure of electrical contacts.

Use of an intermediate barrier layer between the ILD and the copper interconnect permits the successful use of copper in a silicon-based integrated circuit. The barrier layer serves to eliminate the diffusion that would otherwise occur at the copper-ILD junction, and thus prevents the copper from altering the electrical characteristics of the silicon-based semiconductor devices. Such barrier layers are well known in the art and may be formed of a variety of transition metals, transition metal alloys or silicides, metal nitrides, and ternary amorphous alloys. The most common barrier layer materials in use are titanium, tantalum, and tungsten alloys due to their demonstrated ability to effectively reduce copper diffusion.

Deposition of a metallization layer generally occurs through one of the following techniques: chemical vapor deposition (CVD); physical vapor deposition (PVD), also known as sputtering; or electrochemical deposition. CVD involves high temperatures which can lead to cold creep effects and an increased chance of impurity contamination over other methods, and sputtering has problems yielding sufficient step coverage and density at small line widths. Electrochemical deposition, however, offers a more controlled environment to reduce the chance of contamination, and a process that takes place with minor temperature fluctuations. Electrochemical deposition provides more thorough coverage, fewer physical flaws, and reduces separation between the layers.

There are several known electrochemical deposition processes used to form copper interconnects onto barrier layers, each having various disadvantages.

Direct deposition of copper onto the barrier layer typically results in porous films with poor adhesion and inconsistent densities. Annealing of the deposited copper at low temperatures may be performed to improve adhesion, but it increases cold creep effects and fails to provide a consistently dense copper structure. A copper seed layer may be formed over the barrier layer by CVD or PVD to produce an adhesive surface, and then electrochemical deposition may be carried out on the seed layer. This method involves multiple steps and increases production costs by requiring several different types of machines to form each interconnect layer.

What is needed, therefore, is a simple and inexpensive method of forming a metal seed layer that requires only a minimum number of steps for its production.

## SUMMARY OF THE INVENTION

The present invention provides a method of forming a metal seed layer, preferably a copper layer, for subsequent electrochemical deposition. The metal seed layer is formed by the oxidation-reduction reaction of a metal salt or complex such as copper sulfate in acid solution, with a reducing agent such as elemental silicon that is present in a layer on the substrate to be plated. Preferably the reducing agent is present in a sacrificial layer on the substrate. The method is particularly suited to forming metal interconnects for semiconductor devices, because the metal seed layer and the plating of the interconnect itself may be combined into a single-bath operation.

Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.



5

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of a semiconductor wafer undergoing the process of a preferred embodiment of the present invention.

Figure 2 shows the wafer of Fig. 1 at a processing step subsequent to that shown in Fig. 1.

Figure 3 shows the wafer of Fig. 1 at a processing step subsequent to that shown in Fig. 2.

Figure 4 shows the wafer of Fig. 1 at a processing step subsequent to that shown in Fig. 3.

Figure 5 shows the wafer of Fig. 1 at a processing step subsequent to that shown in Fig. 4.

Figure 6 shows the wafer of Fig. 1 at a processing step subsequent to that shown in Fig. 5.

Figure 7 is a cross-sectional view of a semiconductor wafer undergoing the process of a second preferred embodiment of the present invention.

Figure 8 shows the wafer of Fig. 7 at a processing step subsequent to that shown in Fig. 7.

Figure 9 shows the wafer of Fig. 7 at a processing step subsequent to that shown in Fig. 8.

Figure 10 shows the wafer of Fig. 7 at a processing step subsequent to that shown in Fig. 9.

Figure 11 shows the wafer of Fig. 7 at a processing step subsequent to that shown in Fig. 10.

Figure 12 shows the wafer of Fig. 7 at a processing step subsequent to that shown in Fig. 11.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, electrical and chemical changes may be made without departing from the spirit and scope of the present invention.

The terms "wafer" and "substrate" are to be understood as including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. When referring to aqueous solutions described herein, the term "percent" refers to the percent measured by weight, e.g., a 10% hydrofluoric acid solution is 10% by weight hydrofluoric acid. The following description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Referring now to the drawings, where like elements are designated by like reference numerals, an embodiment of the present invention for manufacturing an integrated circuit having a metal interconnect is illustrated by Figs. 1 through 6. The process creates a metal seed layer for subsequent

electrochemical deposition by a oxidation-reduction ("redox") reaction between a reducing agent present in a sacrificial layer of material, and a metal salt or complex. For illustrative purposes the invention is described as a method of plating copper by a reaction in which the reducing agent is silicon, but the use of other metals and reaction mechanisms is to be understood as within the scope of the invention.

The process begins subsequent to the formation of a semiconductor device 20 containing devices 24, which may be transistors, capacitors, word lines, bit lines or the like, and active areas 26 on a silicon substrate 22, as shown in Fig. 1. A protective layer 28 of a material such as borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), or silicon dioxide has been formed over the device 20 by chemical vapor deposition (CVD) or other suitable means.

The process of the present invention begins by applying a photoresist and mask (not shown), and by using photolithographic techniques to define areas to be etched out. Referring to Fig. 2, a directional etching process such as reactive ion etching (RIE) is used to etch through the protective layer 28 to form vias 30. The etchant used may be any suitable etchant that selectively etches the material of the protective layer 28 and not the active areas 26, the devices 24, or the material of sidewall or cap insulators on the devices 24.

Fig. 3 depicts the next step of the process, in which a barrier layer 32 is formed so that it overlies the protective layer 28 and lines the inside of the vias 30. Barrier layers are typically used with metal interconnect material to optimize performance of the interconnects, and to prevent diffusion of the metal interconnect material into the substrate. The barrier layer 32 may be formed of any suitable material such as titanium, titanium nitride, tantalum, tantalum

nitride, tungsten nitride, tungsten-tantalum, tantalum silicon nitride, or other ternary compounds, and should be of a thickness within the range of 50 to 500 Angstroms, and preferably approximately 300 Angstroms thick. Chemical vapor deposition, physical vapor deposition (PVD), or other suitable means may be used to form the barrier layer 32.

Next, a sacrificial oxide layer 34 is formed over the barrier layer 32 and lining the inside of the vias 30, as shown in Fig. 4. The sacrificial oxide layer 34 is a layer of silicon-containing material such as silicon dioxide or silicon monoxide that is formed by means such as CVD, PVD, oxidation of the wafer in an ozone-containing rinse bath, or the like. Preferably the oxide is a chemical oxide. The sacrificial oxide layer 34 has a thickness within the range of 10 to 200 Angstroms, preferably 10 to 50 Angstroms, and should have a silicon-to-oxygen ratio of greater than 0.5. Depending on the reaction mechanism, a sacrificial oxide layer 34 may not be required, and a reactive barrier layer 32 may be used if there is a sufficient amount of the reducing agent present in the barrier layer 32.

Fig. 5 depicts the next step of the process, in which a metal seed layer 36 is now formed on the surface of the barrier layer 32 in the vias 30 by a redox plating process. The plating process is carried out by exposing the wafer 20 to a first plating solution by means such as immersion of the wafer 20 into a plating bath, or by spraying the plating solution onto the wafer 20. The first plating solution is an aqueous solution of an acid such as hydrofluoric acid or sulfuric acid, and a metal salt or complex that is soluble in the acid used. A redox reaction occurs between the metal ions in the solution, e.g., cupric ions ($Cu^{2+}$) and the reducing agent of the sacrificial oxide layer 34, e.g., silicon, leading to reduction of the metal ions and subsequent plating onto the barrier layer 32.

For example, in a copper plating process, a dilute solution of hydrofluoric acid (HF) and a salt such as copper sulfate ($CuSO_4$) is used to carry out the reaction with a sacrificial oxide layer 34 containing silicon as a reducing agent. Preferably a solution containing approximately 1 part hydrofluoric acid per 100 parts water, and about 3 grams of copper sulfate per liter is used, and the reaction is allowed to proceed at room temperature for approximately 2 to 2.5 minutes for a sacrificial oxide layer 34 that is approximately 50 Angstroms thick. The time and temperature may be adjusted as necessary for the thickness of the sacrificial oxide layer 34, and to affect the rate of the reaction. The precise reaction that occurs in the copper plating process is unknown, but is currently believed to be:

$$Si + 2\ Cu^{2+} + 6\ F^- \rightarrow SiF_6^{2-} + 2\ Cu$$

The plating bath in a preferred embodiment is electroless, but an electrolytic bath may also be used. An electrolytic bath permits formation of a thicker metal seed layer 36 than an electroless bath, because electrons are continuously replaced by the electric current applied and therefore the metal ions, which have an electron affinity, may continuously plate to the barrier layer 32. If desired, the plating process may begin as an electroless process, and a voltage may later be applied to carry out an electrolytic plating process.

A conductive layer 38 is now formed in the vias 30 to serve as an interconnect layer, as shown in Fig. 6. The conductive layer 38 is a layer of metal, which may be the same metal as the metal seed layer 36, or a different metal. Preferably the metal seed layer 36 and the conductive layer 38 are layers of the same metal. The conductive layer 38 is formed by an electrochemical deposition process such as electrolytic or electroless plating.

Preferably the conductive layer is formed by exposing the wafer 20 to a second plating solution by means such as immersion of the wafer 20 into a plating bath, or by spraying the second plating solution onto the wafer 20. The second plating solution is typically an aqueous solution of an acid such as sulfuric acid, a metal salt or complex that is soluble in the acid used, and several additives. Either electroless or electrolytic plating, or a combination of the two may be performed as desired for certain applications. In addition, any number of semiconductor wafers may be simultaneously processed by using a large bath, thereby reducing the cost of manufacture.

If the metal seed layer 36 and the conductive layer 38 are formed from the same metal, then the plating process may be carried out in the same plating bath that was used for formation of the metal seed layer 36, and may use the same plating solution. If the metal seed layer 36 and the conductive layer 38 are formed from different metals, then the same tank may be used for both plating processes if the first and second plating solutions are cycled through the tank. Subsequent to the plating process, conventional processing methods, such as planarization of the wafer 20 to isolate the conductive layer 38 into individual contact plugs, may then be used to create a functional circuit from the semiconductor wafer 20.

A second embodiment of the present invention is illustrated by Figs. 7 through 12. Referring to Fig. 7, a semiconductor device 120 contains devices 24, active areas 26, and field oxide regions 40 on a silicon substrate 22. A protective layer 28 has been formed over the device 120, and conductive plugs 42 extend through the protective layer 28 to contact the active areas 26. A protective layer 44 of a material such as BPSG, PSG, BSG, or silicon dioxide has been formed over the device 120 by CVD or other suitable means.

Photolithographic techniques and subsequent etching are then used to define and form a damascene opening or trench 30, as shown in Fig. 8. Referring now to Fig. 9, a barrier layer 32 is now formed so that it overlies the protective layer 44 and lines the inside of the trench 30, as explained with reference to Fig. 3 above. Next, a sacrificial oxide layer 34 is formed over the barrier layer 32 and lining the inside of the trench 30, as shown in Fig. 10, and as further described with reference to Fig. 4 above.

Fig. 11 depicts the next step of the process, in which a metal seed layer 36 is now formed on the surface of the barrier layer 32 in the trench 30 by a redox plating process, as is described further above in reference to Fig. 5. Lastly, a conductive layer 38 is formed in the trench 30 to serve as an interconnect layer, as shown in Fig. 12. The conductive layer 38 is a layer of metal formed by an electrochemical process, as is described more fully with reference to Fig. 6 above. Subsequent to the plating process, conventional processing methods, such as planarization of the wafer 120, may then be used to create a functional circuit from the semiconductor wafer 120.

As can be seen by the embodiments described herein, the present invention encompasses methods of forming a metal seed layer via a redox reaction with a reducing agent. The reducing agent may be present in a sacrificial layer on the substrate to be plated, or may be in a non-sacrificial layer. It should again be noted that although the invention has been described with specific reference to semiconductor wafers, the invention has broader applicability, and may be used in any plating application in which a thin self-limiting seed layer is used.

The above description and drawings are only illustrative of preferred embodiments which achieve the objects, features and advantages of the present

invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is: